IN THE CLAIMS:

Please cancel claims 27 and 28, as shown on the complete list of claims that is presented below.

Claims 1-10 (canceled).

Claim 11 (previously presented). A production process for a semiconductor chip, comprising the steps of:

providing a first internal interconnection and a second internal interconnection on a semiconductor substrate;

forming a surface protective film over the internal interconnections;

forming a first opening and a second opening in the surface protective film to respectively expose a portion of the first internal interconnection and a portion of the second internal interconnection;

forming a bump projecting from the surface protective film on the portion of the first internal interconnection exposed through the first opening, the bump having a side surface; and

forming, after the formation of the bump or simultaneously with the formation of a part of the bump, a surface interconnection that entirely covers the portion of the second internal interconnection exposed through the second opening and that extends to the side surface of the bump to electrically connect the bump to the second internal connection, the surface interconnection having a smaller height than the bump.

Claim 12 (previously presented). A process as set forth in claim 11,

wherein the bump forming step includes the step of selectively depositing a conductive material on the portion of the first internal interconnection exposed through the first opening,

wherein the surface interconnection forming step includes the step of selectively depositing a conductive material in a predetermined region on the surface protective film.

Claim 13 (previously presented). A process as set forth in claim 11,

wherein the conductive material is selectively deposited on the portion of the first internal interconnection exposed through the first opening and in a predetermined region on the surface protective film, thereby to form a part of the bump and the surface interconnection,

wherein the conductive material is further selectively deposited on the part of the bump to complete the bump which projects from the surface protective film.

Claim 14 (previously presented). A process as set forth in claim 11, further comprising the step of forming a recess in a region of the surface protective film on which the surface interconnection is to be formed before the formation of the bump and the surface interconnection, wherein the surface interconnection is formed in the recess.

Claim 15 (previously presented). A process as set forth in claim 14,

wherein the conductive material is selectively deposited in the first opening and the recess to form the part of the bump and the surface interconnection,

wherein the conductive material is further selectively deposited on the part of the bump to complete the bump which projects from the surface protective film.

Claim 16 (previously presented). A process as set forth in claim 15, wherein the selective deposition of the conductive material in the first opening and the recess includes the steps of:

forming a conductive material film over the surface protective film having the first opening and the recess; and

removing the conductive material film except portions thereof in the first opening and the recess.

Claim 17 (previously presented). A process as set forth in claim 16, wherein the removal of the conductive material film includes the step of partly polishing away the conductive material film except the portions thereof in the first opening and the recess for planarization thereof.

Claim 18 (previously presented). A process as set forth in claim 16, wherein the removal of the conductive material film includes the step of entirely polishing away the conductive material film except the portions thereof in the first opening and the recess for planarization thereof.

Claim 19 (previously presented). A process as set forth in claim 14, wherein the recess has a bottom surface located at a lower level than a top surface of the internal interconnection.

Claim 20 (previously presented). A process as set forth in claim 14, further comprising the step of planarizing a surface of the surface protective film after forming the surface protective film and before forming the first opening and the recess.

Claim 21 (previously presented). A process as set forth in claim 11, wherein the bump includes a peripheral bump to be provided outside a device formation region of a semiconductor substrate which is a base body of the semiconductor chip.

Claim 22 (previously presented). A process as set forth in claim 21, wherein the peripheral bump is configured as surrounding the device formation region.

Claim 23 (previously presented). A process as set forth in claim 21, wherein the peripheral bump is formed in a scribe line region.

Claim 24 (previously presented). A process as set forth in claim 21, wherein the surface interconnection is formed to be connected to the peripheral bump.

Claim 25 (previously presented). A process as set forth in claim 11, wherein the step of forming a surface interconnection comprises electroplating with material for the surface interconnection.

Claim 26 (previously presented). A process as set forth in claim 11, wherein the step of forming a surface interconnection is conducted so that the surface interconnection has a substantially uniform thickness.

Claims 27 and 28 (canceled).